42. (New) The integrated circuit device according to claim 41 further comprising at least one lead coupled with the semiconductor die and the housing encapsulates at least a portion of the at least one lead.

43. (New) The integrated circuit device according to claim 41 wherein the heat sink comprises:

a body; and

at least one lead coupled with the body and configured to dissipate heat from the semiconductor die externally of the housing.

44. (New) The integrated circuit device according to claim 43 wherein the housing encapsulates at least a portion of the at least one lead.

45. (New) The integrated circuit device according to claim 41 wherein the housing encapsulates substantially an entirety of the heat sink.

46. (New) The integrated circuit device according to claim 41 wherein the housing surrounds the heat sink and the semiconductor die.

47. (New) The integrated circuit device according to claim 41 wherein the housing encapsulates the semiconductor die.

48. (New) An integrated circuit device comprising:

a housing enclosing a semiconductor die comprising memory circuitry; and

a heat sink positioned in heat-receiving relation with the semiconductor die and configured to release heat outside the housing.

49. (New) The integrated circuit device according to claim 48 wherein the heat sink comprises at least one lead configured to conduct heat externally of the housing.

50. (New) The integrated circuit device according to claim 48 wherein the housing forms one of a vertical surface mounted package and a horizontal surface mounted package.

51. (New) The integrated circuit device according to claim 48 wherein the housing comprises a first housing enclosing the semiconductor die and a second housing enclosing the first housing and at least partially enclosing the heat sink.

52. (New) The integrated circuit device according to claim 48 wherein the housing comprises a first housing enclosing the semiconductor die and a second housing enclosing the first housing and the heat sink.

53. (New) An integrated circuit device comprising:

a first lead frame;

a semiconductor die secured to the first lead frame;

a second lead frame comprising a heat sink thermally coupled with the semiconductor die; and

a housing formed about at least portions of the semiconductor die and heat sink.

54. (New) The integrated circuit device according to claim 53 wherein the housing comprises an encapsulant housing.

55. (New) The integrated circuit device according to claim 53 wherein the semiconductor die comprises memory circuitry.

56. (New) The integrated circuit device according to claim 53 wherein the housing is configured to provide portions of the first lead frame and second lead frame outwardly exposed relative to the housing.

57. (New) The integrated circuit device according to claim 56 wherein the housing comprises a plurality of sides, and wherein the portions of the first and second lead frames extend from the same side.

58. (New) The integrated circuit device according to claim 53 wherein the portions of the first and second lead frames are bent to provide horizontal mounting of the integrated circuit device.

59. (New) The integrated circuit device according to claim 53 wherein the housing forms one of a vertical surface mounted package and a horizontal surface mounted package.

Q2

60. (New) The integrated circuit device according to claim 53 wherein the housing encapsulates an entirety of the semiconductor die.

61. (New) The integrated circuit device according to claim 53 wherein the housing encapsulates an entirety of the semiconductor die and the heat sink.